REMARKS

Claims 1-30, all the claims pending in the application, stand rejected.

Claim Rejections - 35 DSC § 102

Claims 1, 3-7, 9-11, 13, 14, 16, 18, 19, 22-24, 26, 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (Pub No. US 2003/0160235 Al). This rejection is traversed for at least the following reasons.

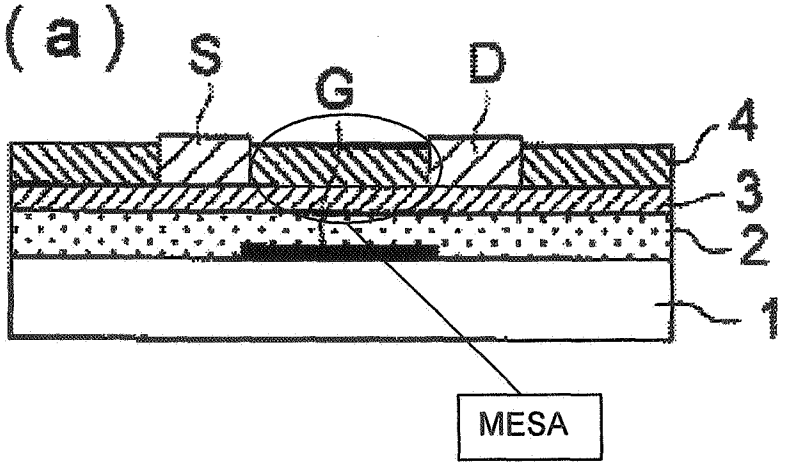
Claim 1

Independent claim 1 is directed to a thin film transistor electronic switching device having source and drain electrodes with a semiconductor region therebetween, a gate electrode and an insulating region located between the source and drain electrodes. The insulating region is "configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is **greater than** the shortest physical distance between the source and drain electrodes."

Hirai et al

The Examiner asserts at page 3 of the Office Action that Figure 1(a) of Hirai shows an electronic switching device in which the length of the shortest current path between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes. However, Figure 1(a), reproduced below, clearly shows a configuration in which the shortest physical distance between the source and drain electrodes is also the length of the shortest current path: along the interface between insulation layer 4 and semiconducting region 3.

FIG. 1 (a)



No Teaching of Length in Hirai et al

In the thin-film transistor described in Hirai and shown in Figure 1(a), charge carriers travel in semiconducting layer 3 at the interface with insulation layer 4. The Examiner does not provide any support for the assertion that the length of the shortest current path between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes in Hirai. The Examiner is merely speculating, without proof as to the relevant distances. The difference in distances is not inherent, as the clear structure, as understood by one skilled in the art, would be a current path that is equal to the physical distance.

Hirai et al does not discuss the nature of the semiconductor/insulator interfaces it describes. Specifically, Hirai et al does not teach that such interfaces might be irregular on any scale. There is no explicit or implied disclosure in Hirai of the concept of arranging an insulating region between source and drain electrodes so as to cause the length of the shortest current path between the electrodes to be greater than the shortest physical distance. Claim 1 is therefore novel over Hirai et al.

Atomic Differences are Not Contemplated by Claim 1

Applicants note that the Examiner might assert that there is a difference on an atomic scale. However, such position is unsupported since there is no discussion in Hirai et al as to atomic scale distances. Furthermore, Applicants submit that the skilled person in this art would understand that claim 1 is distinguished over a device in which an atomically irregular semiconductor/insulator interface makes the calculation of the length of the current path difficult.

Finally, Applicants had expressly distinguished the invention over prior art similar to Hirai et al on greater than an atomic level and has, thus, disclaimed such interpretation as of the filing of the application.

Invention Expressly Distinguished Over the Prior Art

The transistor architecture shown in Figure 1(B) of the present application has the same configuration as shown in Figure 1(a) of Hirai, in the sense that the shortest current path between the source and drain is along the semiconductor/insulator interface. This is to be contrasted with the transistor architecture of the present invention shown in Figures 1(C) and 1(D). The transistor architectures of Figure 1 are discussed at pages 8 and 9 of the present application and, in particular, states that in the conventional transistor architecture shown in Figure 1(B) the shortest current path and the shortest physical distance between the source and drain electrodes are equal in length. That same discussion states that for Figures 1(C) and 1(D), L_{SC} is longer than LSD. Claim 1 is consistent and recites that the length of the shortest current path is greater than the shortest physical distance between the source and drain electrodes. Thus, it is clear that the scope of claim 1 does not include devices of the configuration disclosed in Hirai et al.

Evidence of Performance Differences

Figure 3 of the present application shows two switching devices made to the designs depicted in Figures 1(B) and (C), and the transfer characteristics of those devices. Device A has a structure known in the art (see page 5, paragraph 3) and has the same configuration as shown in Hirai, Figure 1(a) – device A is simply inverted, being a top-gate device. Device B is a device manufactured in accordance with the present invention and has an insulating mesa between the source and drain electrodes so as to cause the length of the shortest current path to be greater than the shortest physical distance between the electrodes.

Given the identity between Figure 1(a) of Harai et al and Figure 1(B) in the present application, a device made to the design depicted in Figure 1(a) of Hirai et al would have the same atomic path as for the device A, which is fabricated by a solution-based technique. Applicants expressly distinguished device A in Figure 3, as illustrated in Figure 3. Thus, given applicable standards for claim interpretation, a person skilled in the art would conclude that the term "greater than" in claim 1 does not specify the relative lengths of the current path and

physical separation of the electrodes to atomic accuracy. Claim 1 is distinguished over both device A and any device made to the design depicted in Figure 1(a) of Hirai by the limitation that the shortest current path is greater in length than the shortest physical distance between the source and drain electrodes of the device. The present application is not concerned with irregularities at the atomic level and, from graphs C and D of Figure 3, it is further clear that mere atomic irregularities at a semiconductor/insulator interface do not confer the advantages of the present invention.

Claim 18

Independent claim 18 is directed to a method for forming a thin film transistor electronic switching device, including formation of a source electrode, a drain electrode, a semiconducting region in contact with and extending between the source and drain electrodes, gate electrode disposed for influencing the transconductance of at least part of the semiconducting region; and an insulating region located between the source and drain electrodes. The claim expressly states that the formation steps result in the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeding the shortest physical distance between the source and drain electrodes.

Because of the limitation to the respective lengths being different, as with claim 1, this method claim would be patentable over Hirai et al, taken alone or in combination with other cited art.

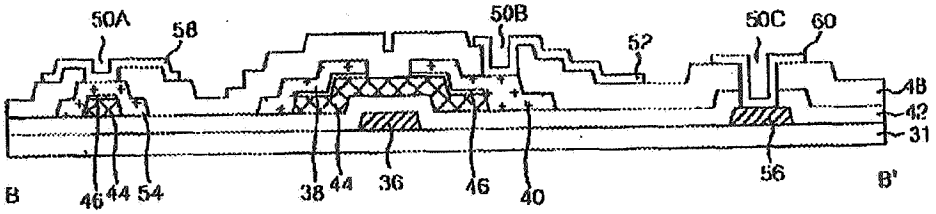
Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Hirai et al. as evidenced by Konstantinos et al. (Japanese Pub No. 2000-260999, hereinafter Konstantinos et al.). This rejection is traversed for at least the following reasons.

The distinction over Hirai et al is clear, and Konstantinos does not evidence how Harai can be viewed on a non-atomic level to meet the limitations of parent claim 1 or claim 8.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Choi et al. (Pub No. US 2002/0084459 A1, hereinafter Choi et al.). This rejection is traversed for at least the following reasons.

The Examiner asserts that Figure 5 of Choi describes the same configuration of source and drain electrodes with respect to the semiconducting layer as in Hirai. The Examiner asserts that the shortest current path between source electrode 38 and drain electrode 40 lies in semiconducting layer 44, along the interface with insulator 48.

FIG.5



However, at pages 8 and 9 of the present application, Applicants describe the advantages of an electronic switching device configured in accordance with the present invention. By including an insulating region (such as the mesa of device B) between the source and drain electrodes, the flow of leakage currents between source and drain electrodes is suppressed and the OFF current of the switching device is greatly reduced. This novel device architecture provides short-channel transistors with a greater ON-OFF current ratio, allowing viable thin-film transistors to be fabricated with submicrometer channel lengths.

Choi et al does not teach or suggest that an insulating region may be located between source and drain electrodes so as to improve the ON-OFF current ratio of a switching device. Indeed, as a concept it is counter-intuitive that including a further insulating region should improve the ON-OFF current ratio of a switching device, since it is natural to expect that the presence of the additional insulator would decrease the ON current and that the increased interfacial area would increase the concentration of defects in the adjacent semiconductor region, and hence the leakage current.

Claim Rejections - 35 U.S.C. § 103

Claims 2 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to claim above. This rejection is traversed for at least the following reasons.

The Examiner asserts that with regards to dependent claims 2 and 17, Hirai et al. teaches the limitations of claim I for the reasons above. The Examiner admits that Hirai et al. does not teach a shortest current path through the semiconductor region between the source and drain to be greater than 1.05 times the shortest physical distance between the source and drain, nor does it teach a physical distance between the source and drain to be less than one micrometer. The Examiner asserts that on the basis of the teachings of the references, it would have been obvious to determine the optimum shortest current path or physical distance between the source and drain electrodes (citing *In re Aller, Lacey, and Hall*, 10 USPQ 233-237).

The Examiner's rejection necessarily relies on the premise that the use of distances that are different at greater than an atomic level would be obvious. Applicants have demonstrated that the art teaches in the opposite direction, and thus have demonstrated that the Examiner has not made a *prima facie* case of obviousness under the applicable Guidelines subsequent to the KSR decision. The burden is on the Examiner to demonstrate facts that would overcome the strong case developed by Applicants showing that Applicants invention is novel and unobvious.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to claim 1 above, and further in view of Han et al. (Pub No. US 2003/0155572) This rejection is traversed for at least the following reasons.

The Examiner asserts that Hirai et al. teaches the limitations of claim 1 for the reasons above, but admits that Hirai et al. does not teach an insulating region to comprise of an air gap. The Examiner looks to Han et al for a teaching as to how incorporating air gaps will reduce heat transmission along a vertical direction because it has low thermal conductivity (see ¶ 24, lines 11-12,16-17).

However, Han et al does not teach one skilled in the art away from the equal path lengths contemplated by Hirai et al. Thus, in the absence of such teaching, the claim would be patentable.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et, al. as applied to claim 18 above. This rejection is traversed for at least the following reasons.

The Examiner admits that Hirai et al. does not teach the thickness of the insulating region to be in the rage of 30 to 80 nm. However, the Examiner asserts that, given the teaching of the

references, it would have been obvious to determine the optimum thickness of the insulating region (citing *In re Alter, Lacey, and Hall* (10 USPQ 233-237).

However, neither the knowledge of one skilled in the art (because the invention goes contrary to the convention in the art) nor the cited references teach one skilled in the art away from the equal path lengths contemplated by Hirai et al. Thus, in the absence of such teaching, the claim would be patentable.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to claim 18 above, and further in view of Berger et al. ("Projection electron-beam lithography: A new approach, S.D. Berger, J.M. Gibson, R.M. Camarda, hereinafter Berger et al.). This rejection is traversed for at least the following reasons.

The Examiner asserts that Hirai et al. teaches the limitations of claim 18 for the reasons above and admits that it does not teach forming one or more components of the device using electron beam lithography. The Examiner looks to Berger et al. for a teaching of how electron beam lithography offers high resolution, high throughput, and good overlay and registration characteristics (citing Abstract, lines 1-3).

However, neither cited references teaches one skilled in the art away from the equal path lengths contemplated by Hirai et al. Thus, in the absence of such teaching, the claim would be patentable.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al as applied to claim 18 above, and further in view of David Grewell, Abbass Mokhtarzadeh, Avraham Benaar ("Feasibility of Selected Methods for Embossing Micro-features in Thermoplastics", ANTEC 2003, May 4-8, 2003, hereinafter Grewell et al). This rejection is traversed for at least the following reasons.

The Examiner asserts that Hirai et al. teaches the limitations of claim 18 for the reasons above and admits that it does not teach using embossing techniques to forming the insulating region. The Examiner looks to Grewell et al. for a teaching of how embossing techniques are utilized since they have the capability to produce features 10 micrometers in width or even in sub-micron range (citing Introduction, lines 1-9).

However, neither cited references teaches one skilled in the art away from the equal path lengths contemplated by Hirai et al. Thus, in the absence of such teaching, the claim would be patentable.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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